15 Outside the Electron

15.1 Introduction to expanding the Electron

This chapter is intended for those who want to add their own bits of hardware onto the Electron. There are several reasons for doing this. The most common one is to allow the Electron to access facilities provided for the BBC Micro. All of the common interfaces such as discs, printer port, analogue to digital converter, speech chip, paged ROMs etc. can easily be added onto the Electron. If care is taken with the design, these products will operate in an almost identical manner to those on the BBC Micro. Several interface addons can already be purchased from Acorn.

If the only point in adding hardware onto the Electron were to make it totally BBC Micro compatible, there would have been little point in buying the Electron in the first place. In fact, the Electron has more potential for expansion than a BBC Micro. Why? Because all necessary system buses come out on the expansion connector. This ability to access all of the buses means that the devices which can be added onto the Electron are limited only by the imagination (and maximum allowable loading of the buses).

15.2 The Expansion Connector

All required signals from the Electron are present on this connector. In order to make use of them, a basic knowledge of interfacing to the 6502 will be required. Such a knowledge can be acquired by reading some of the popular electronics magazines and specialised books on interfacing. The aim in this book is to explain all of the details to those who have already read enough about microcomputer hardware in general, and now want to know about the Electron in particular.

Bottom			Top
18V AC	2	1	18V AC
AC RETURN	4	3	AC RETURN
-5V	6	5	-5V
0V	8	7	0V
+5V	10	9	+5V
16MHz	12	11	SOUND O/P
PHI OUT	14	13	÷13 IN
$\overline{\text{NMI}}$	16	15	$\overline{\text{RST}}$
R/$\overline{\text{W}}$	18	17	$\overline{\text{IRQ}}$
D6	20	19	D7
D4	22	21	D5
D2	24	23	D3
D0	26	25	D1
NC	28	27	$\overline{\text{RDY}}$
SLOT	30	29	SLOT
A14	32	31	A15
A12	34	33	A13
A10	36	35	A11
A0	38	37	A9
A2	40	39	A1
A4	42	41	A3
A6	44	43	A5
A8	46	45	A7
0V	48	47	0V
+5V	50	49	+5V

Figure 15.1 - Expansion connector layout

18V AC (pins 1 ,2)

>These lines are connected directly to the output
>from the Electron mains power adaptor.

AC return (pins 3,4)

>Up to 6 watts of power may be drawn from this
>source (provided that none is drawn from the +5V
>line). Bear in mind that the AC will have to be
>rectified and smoothed before it can be used to
>drive any computer chips.

–5V pins (5,6)

> This is a -5 volt supply from the Electron, from which a maximum of 20mA can be drawn. It would often be used to power RS423 expansions.

0V (pins 7,8,47,48)

> This is the signal and power ground on the Electron. All external circuits must have their 0 volt lines connected to this point.

+5V (pins 9,10,49,50)

> This is a +5 volt power supply from the Electron. A maximum of 500mA can be drawn from it, but note that no power can be taken from the 18V AC line if this is done.

Sound o/p (pin 11)

> Sound output from the Electron ULA. This signal is 3 volts peak to peak fed via a 1K series resistor.

16 MHz (pin 12)

> This is the master 16 MHz clock from the Electron main oscillator. It can be used for clock generation on expansion modules, but see section 15.3.3 for a description of clock synchronisation.

16/13 MHz (pin 13)

> This is 16 MHz divided by 13. It is normally used for baud rate generation, and will give approximately 1200Hz if divided by 1024.

PHI out (pin 14)

> This is a nominally 2 MHz clock as connected to the 6502A. The low time is some 250ns. The high time varies depending upon the operation being performed. It is 250ns when reading ROMs, 750ns or 1250ns when accessing the 1MHz bus (depending upon the relative phase of the 2MHz clock) and can be up to 40us due to screen access in modes 0 to 3. The clock timing is covered in greater depth in section 15.3. Note that the NMI must be synchronised with PHI out. This is because the NMIs give the 6502 precedence over the ULA for the RAM. Incorrect data may be read from the RAM if the NMI is not latched on a negative going edge of PHI out.

RST (pin 15)

> Active low reset signal. This is an OUTPUT ONLY for reseting expansion modules on power up, or when the BREAK key is pressed.

NMI (pin 16)

> Non-maskable Interrupt (negative edge triggered). This open collector (wire-OR) line is the system NMI and can be asserted by an expansion module pulling it low. There is a 3K3 pull-up resistor inside the ULA. You must be very careful to avoid holding this line low after the interrupt has been serviced, because it will mask other interrupts whilst asserted. For more details about NMIs, you should refer to chapter 7.

IRQ (pin 17)

> This is the active-low IRO (interrupt request). It is an open collector (wire-OR) line, so it can be asserted by any expansion module pulling it low. There is a 3K3 pull-up resistor within the ULA. Note that interrupts MUST NOT occur until the

software in the machine has initialised to a state at which it can deal with them. Power up and reset conditions should therefore disable all IROs, It is important to ensure that not too much of the interrupt service time is used up, otherwise some operations like the system clock may cease to function correctly.

R/W (pin 18)

This is the system read/write line from the 6502. It tells peripheral devices whether the 6502 is sending data to them, or is expecting data from them.

D0-D7 (pins 19 to 26)

This is the 8 bit wide bi-directional data bus. All data is transferred over this bus, the direction of data transfer being determined by the state of the read/write line.

RDY (pin 27)

This is the active low ready line from the 6502. It can be asserted by an expansion to slow down the processor when it is reading slow memory. This line is only operational on reads.

(pin 28)

No connection.

(pins 29,30)

Polarising key connector to ensure that boards cannot be plugged in the wrong way round.

A0-A15 (pins 31 to 46)

This is the system address bus. There are 16 lines in this bus which allow 216 (65536) different locations to be addressed.

15.3 Designing Circuits

It might at first appear to be very easy to add anything onto the Electron Expansion Bus. There is however one fairly major problem. The 6502A often changes speed to cope with the accessing of different devices. These fall into two main categories.

15.3.1 Accessing the ROM

When the ROM is being accessed, the 6502 runs at the maximum possible speed of 2MHz; PHI OUT is low for 250ns and then high for 250ns.

15.3.2 Accessing the RAM and peripherals

When RAM or peripheral devices are accessed, the timing will be highly dependent on the display mode. This is because twice as much data has to be removed from the RAM to produce the display in modes 0–3 as in modes 4–6.

Modes 4–6

The processor will normally be running at 2MHz when it first needs to access RAM or peripherals like the 6522. It has to slow down to 1MHz first. This *slow down* either consists of a PHI OUT low time of 250ns followed by a high time of 750ns, or a low of 2SOns followed by a high of l2SOns. The particular type of transition which occurs will depend upon the relative phases of the 2MHz and 1MHz clocks, This is illustrated in figure 15.1. Both the 1MHz and 2MHz clocks are *internal* to the ULA, and are not available outside. They must be generated separately (see later in this section).

Modes 0–3

In these modes, the ULA must have access to the RAM for all the displayed part of a line (40us out of 64us in 256 lines out of 312). This doesn't matter provided that the CPU only wants to access peripherals and the ROM, which it is free to do in the normal way. However, if it tries to access RAM the the ULA will hold it's clock high for up to 4Ous. The overall effect is that the processor

can be effectively disabled for up to 40us. The only way for the processor to obtain priority over the ULA is by an NMI being generated. This will automatically cause the ULA to release the 6502 (and the RAM), but inevitably creates snow on the screen.

15.3.3 Generating the 1MHz clock

Since the 1MHz and 2MHz signals only exist inside the ULA, it is necesary to regenerate them outside. Two clocks are provided on the expansion connector. A 16MHz one and a 16/13MHz one for baud rate generation. The former of these can be used to generate a 1MHz clock, This has to be synchronised to the processor clock if it is to be used with peripherals like the 6522 VIA. A simple division by 16 will not produce a suitable clock signal. The circuit in figure 15.2a will produce a suitable in phase signal. The timing for this is shown in figure 15.2b.

15.3.4 Long delays for interrupts

It is important to bear in mind how long the delays might be before a particular requested interrupt is serviced, This is determined by the longest period for which interrupts can be disabled.

In modes 0−3, this delay can be up to 10ms in the very worst case. Such a long delay can cause problems with unbuffered circuits like the cassette serialiser/deserialiser. The only solution is to ensure that such devices are only used from modes 4−6 (even if it means forcing a particular mode before executing a routine).

The interrupt delay is only 4ms at worst in modes 4−6, so most actions which require a fast response can be executed in one of these modes. Note that NMIs can always be used as a last resort where necessary, but are normally reserved for disc and Econet accesses.
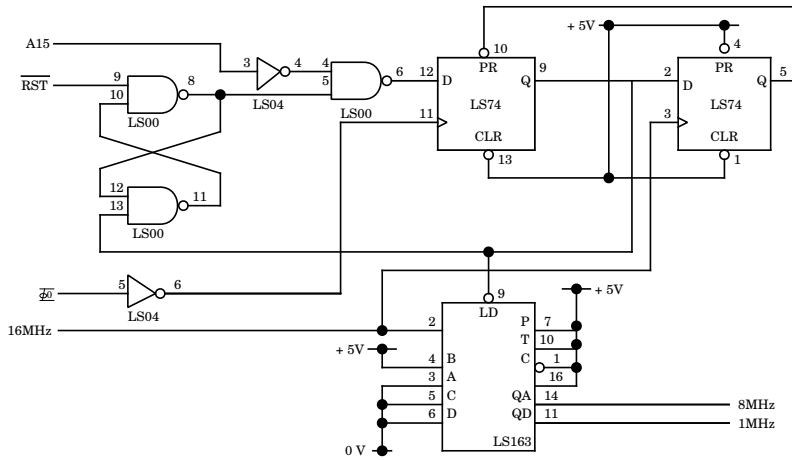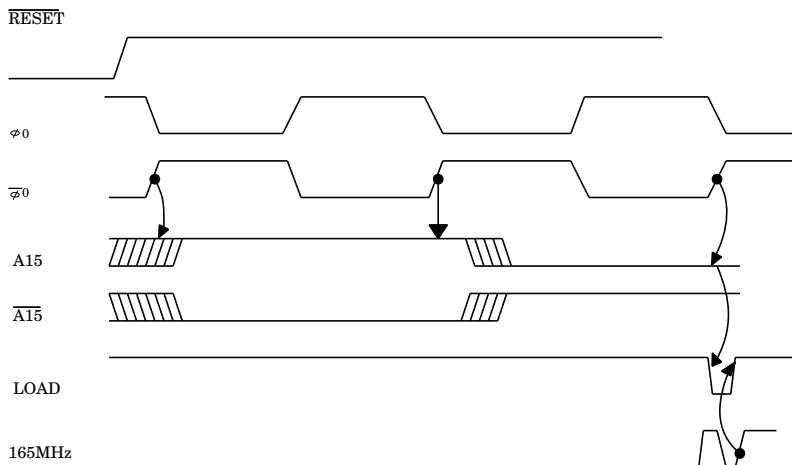
Figure 15.2a - A 16MHz to 1MHz synchronisation circuit

Figure 15.2b - the timing applied to figure 15.2a

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15.4 Sideways ROMs

Sideways ROMs can be selected in place of BASIC. Languages like LISP, disc filing systems, utilities etc can all be plugged in. These sideways ROMs are covered from a software point of view in chapters 8 to 11.

From a hardware point of view, up to 16 sideways ROMs ae allowed. However, four of these are already allocated on the standard Electron. BASIC occupies two slots (ROMs 10 and 11 it appears the same in each). The *keyboard* occupies slots 8 and 9. The remaining 12 ROM slots are all available for expansion.

The ROM paging register is located in the ULA, and can be accessed by writing to location &FE05 (see section 14).

There are two distinct ways of accessing ROMs via this register. The first method accesses ROMs 12 to 15. This operation is very simply performed by writing the required ROM number into the low nibble of &FE05. Hence:

```
                D7  D6  D5  D4  D3  D2  D1  D0
Write at &FE05  0   0   0   0   1   1   R1  R0
```

where R1 and R0 control which ROM is selected.

Suitable hardware must be included in the expansion unit to cope with this method of selecting ROMs. Selection of one of the ROMs 12 to 15 can be carried out by the following code. Be careful to ensure that the write to &F4 always occurs before the write to &FE05, just in case an interrupt occurs in between.

```
LDA #ROMnumber
STA &F4
STA &FE05
```

The second method for accessing ROMs will allow those numbered 0 to 7 to be selected. It is not possible to select these ROMs directly, because BASIC will still be paged in. The only way of paging BASIC and the keyboard out is to select one of the ROMs 12 to 15 first. This access causes the internal ROMs to page out. The correct ROM selection code can then be sent to the lower three bits of &FE05.

	D7	D6	D5	D4	D3	D2	D1	D0
Write at &FE05	0	0	0	0	1	R2	R1	R0

where R2, R1 and R0 select the required ROM.

As with the other ROM slots, new hardware must be provided at address &FE05 to select the relevant ROMs. Code to select a ROM numbered 0 to 7 could be:

```
LDA    #&0C          \to deselect BASIC
STA    &F4           \one of ROM 12 to 15
STA    &FE05         \must be selected
LDA    #ROMnumber    \Now select desired
STA    &F4           \low order ROM
STA    &FE05
```

It is essential that the A register is stored to &F4 before &FE05 in case an interrupt occurs in between.

When the machine is powered up, the sideways ROMs are polled in order from 15 down too. The first one which is found to be a language ROM (see the Paged ROM firmware section for specification) will start executing. Since BASIC is in slot 10/11, a ROM which is required to power-up before BASIC must be in one of the sockets 12 to 15.

The ROMs 12 to 15 are allocated to high priority NMI devices or languages which are expected to power up before BASIC. The reason for putting high priority NMI servicing ROMs in these sockets is that a smaller delay is required to page them in than for ROMs 0 to 7.

The lower priority ROMs are all selected by performing two writes to the paging register. The first is to deselect BASIC, the second is to select the required ROM.

The Acorn Plus 1 expansion unit forces the priority of ROMs to be (from highest down):

> ROMs 15 to 12
> ROMs 7 to 0
> BASIC

This implies that any language which is fitted to the Plus1 will automatically power up ahead of BASIC. ROM allocation has been defined by Acorn as follows:

ROM USE

0,1   Second external socket on expansion module (SK2)
2,3   First external socket on the expansion module (SK1)
4   Disc
5,6   USER applications
7   Modem interface ROM
8,9   Keyboard
10,11 BASIC
12   Expansion module operating system
13   High priority slot in expansion module
14   ECONET
15   Reserved

15.5 The One Megahertz Bus

Most 6502 compatible peripherals will generally be connected onto the 1MHz regenerated bus. This allows relatively slow devices to be accessed. On the BBC Micro, page &FC has been allocated especially for 1MHz devices, This page is called FRED. Generally, devices resident within FRED have relatively small memory requirements (mainly control and data registers).

Since Electron expansion should be compatible with BBC Micro expansion (so they can use the same expansion peripherals), the allocation of devices in FRED has been very well defined. The following list includes items which would normally be resident in Sheila on the BBC Micro, but which have to go on the 1MHz bus on an Electron.

The initial allocations of space are:−

&FC00 to &FC0F	Test hardware
&FC10 to &FC13	TELETEXT
&FC14 to &FC1F	PRESTEL
&FC20 to &FC27	IEEE 488 interface
&FC28 to &FC2F	ECONET
&FC30 to &FC3F	CAMBRIDGE RING interface
&FC40 to &FC47	WINCHESTER DISC interface
&FC48 to &FC5F	Reserved for Acorn expansions
&FC60 to &FC6F	6850 ACIA
&FC70	A to D converter
&FC71	CENTRONICS parallel interface
&FC72	Status register
	BSY ADC FB2 FB1 X X X X

Where   BSY = printer busy
         ADC = A to D conversion end
         FB1 = Fire button 1
         FB2 = Fire button 2
         X = undefined

&FC73 to &FC7F	Reserved for Acorn expansions
&FC80 to &FC8F	Test hardware
&FC90 to &FC9F	Sound and speech
&FCA0 to &FCAF	Reserved for Acorn expansions
&FCB0 to &FCBF	6522 VIA/Real time clock
&FCC0 to &FCCF	Floppy disc controller
&FCD0 to &FCDF	USER applications
&FCE0 to &FCEF	The TUBE
&FCF0 to &FCFE	USER applications
&FCFF	Paging register for JIM

Note that page &FD in the Electron address space is used in conjunction with the paging register in FRED to provide an extra 64K of memory. This memory is accessed one page at a time. The particular page being accessed is selected by the value in FRED's paging register, and is referred to as the *extended page number*. Accessing memory via the 1MHz bus in this way will generally be about 20 times slower than accessing memory directly.