DICE WARNING

Because the 6502 has a pipelined instruction fetch, decode and execute, the fetching of the next instruction is already under way before the current instruction has completed execution. The DICE 6502 has the same characteristic, which can cause peculiarities when a Breakpoint is set immediately following a Branch instruction; the Breakpoint will be hit regardless of whether the branch succeeds or not, due to the instruction fetch occurring on the Breakpoint Instruction before the Branch has completed execution.

The symptoms of a breakpoint being hit in this manner are the apparently incorrect contents of the Program Counter after hitting the Breakpoint; the PC will contain the address of the Branch destination, rather than the instruction immediately following the Breakpoint, although in cases where the two are the same, the user may not realise that the breakpoint has been incorrectly encountered, unless he/she checks the Flags against the branch condition.

e.g. A program contains the following instruction sequence:

```
E38E            BEQ     E39B
E390            LDX     £0      <-- Breakpoint set at E390
::::            :::     ::::
E39B            LDA     £4
```

On executing the BEQ at E38E with the Z flag set (i.e. the branch WILL take place), the breakpoint at E390 will be hit due to the instruction pre-fetch, and the DICE will halt showing PC=E39B and Z=1, i.e. the branch did take place.

This situation has not been examined for all cases of non-linear code, although JSRs do not appear to cause the problem when a Breakpoint is set at the immediately following instruction.

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